IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of: Group Art Unit: 1775

Applicant: Matthias Oechsner Examiner: McNeil, Jennifer C.

Serial No.: 10/087,716 Atty. Dkt.: 01P05135US01

#5
10/18/03
AS

Filed: March 1, 2002

Title: THERMAL BARRIER COATING HAVING SUBSURFACE INCLUSIONS FOR IMPROVED THERMAL SHOCK RESISTANCE

Assistant Commissioner for Patents
P.O. Box 1450
Washington, DC 20231-450

DECLARATION OF RAMESH SUBRAMANIAN
UNDER 37 CFR 1.132

1. I, Ramesh Subramanian, a citizen of India, hereby declare and state as follows:

2. I have been continuously employed by Siemens Westinghouse Power Corporation and its predecessor, Westinghouse Electric Corporation, for approximately the past six years. I am currently Coatings Group Leader in the Materials Department, and I work in the field of high temperature ceramic materials and coatings.

3. Prior to my employment by Westinghouse Electric Corporation, I was employed by the Department of Energy at the Oak Ridge National Laboratory for approximately two and one-half years, working in the field of high temperature materials.

4. I received a doctorate degree (PhD) in Materials Science from Cornell University in 1995. My combined academic and commercial experience in the field of materials science totals approximately fifteen years.

5. I understand that the USPTO Examiner has rejected all claims in the above-cited application on the basis that the claimed invention is anticipated by the teaching of Freling (US patent 6,190,124) and Seals (US patent 6,071,628). I understand that the Examiner's position is that prior art products

produced in accordance with these references will necessarily or inherently possess characteristics of the claimed invention.

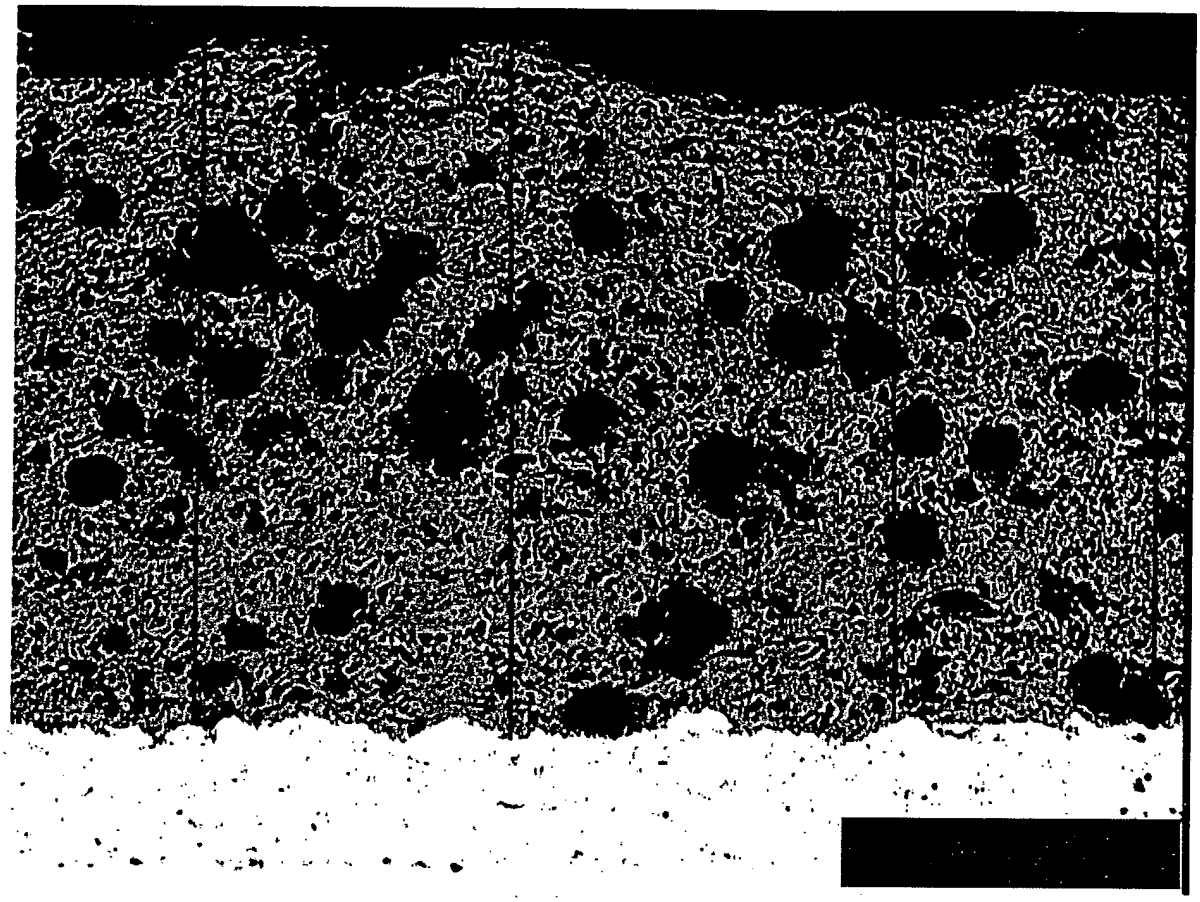
6. On information and belief, I disagree with the Examiner's position that the abradable seal surface material 30, 36 of Freling will have voids with cracks that extend between the void and the surface of the ceramic coating. The attached photomicrograph, provided in both full color and black and white versions for the Examiner's convenience, shows one such ceramic coating at a magnification of 50X. The coating illustrated is a common zirconium oxide stabilized with about 8 wt.% yttrium oxide having voids created with a fugitive polymer material, as described in prior art patent 4,936,745. The voids are visible as dark blotches within the lighter color (orange-brown) ceramic material. Notice that there are no cracks extending between the voids and the surface (visible at the top of the photo). This photomicrograph is representative of all such coatings that I am familiar with. Accordingly, it is not necessary or inherent that thermal barrier coated components have voids with cracks that extend between the void and the surface of the ceramic coating.

7. On information and belief, I disagree with the Examiner's position that the thermal barrier coating 7 of Seals will have voids with cracks that extend between a void and the surface of the ceramic coating. The Examiner points to the teaching of Seals that the material will contain microcracks. However, such microcracks are known to form in a ceramic material deposited by a thermal process due to stresses caused during the cooling of the material. Such microcracks are known to be randomly oriented and not necessarily or inherently extending from embedded hollow structures to the free surface. Should one or more of these random microcracks extend to make contact with an embedded hollow structure, the crack would still contain a crack tip at its opposed end, and may include a second crack tip that extends around the embedded hollow structure. Accordingly, it is not necessary or inherent that thermal barrier coated components have voids with cracks that extend between the void and the surface of the ceramic coating.

8. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or of any patent issuing there from.

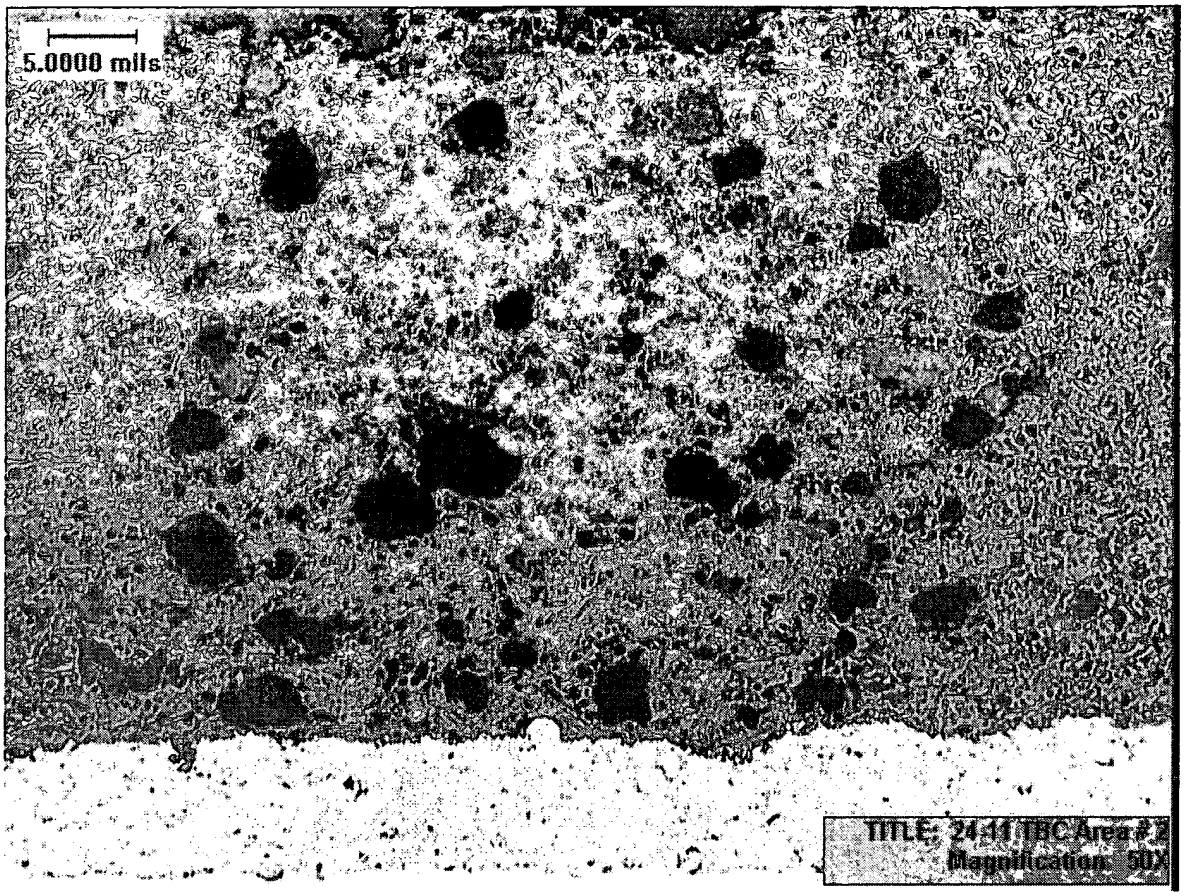
Dated: 10/03/03 By: _____

Ramesh Subramanian



ATTACHMENT TO:

DECLARATION OF RAMESH SUBRAMANIAN
UNDER 37 CFR 1.132



ATTACHMENT TO:

DECLARATION OF RAMESH SUBRAMANIAN
UNDER 37 CFR 1.132